Amendments to the Specification:

On page 2, please replace paragraph **[0005]** with the following amended paragraph:

[0005] Given that a FIFO storage circuit has a limited storage size, provisions have been made in the prior art in case of an overflow condition in the FIFO. Such an overflow occurs when a data word is received or otherwise scheduled to be written into the FIFO, yet the writing of that word would overwrite valid data in the FIFO that has not yet been read. In other words, were such a word written into the FIFIO, it would overwrite and thereby destroy valid data. In the prior art, when such a potential overflow is detected, then some type of intervention has been employed. A common response is to prevent the write, which would otherwise overwrite valid unread data, while also generating an interrupt to some type of controller or other responsive circuit. In this way, the responsive circuit can deny the receipt of any additional words while also holding the FIFO write in abeyance until a read from the FIFO occurs, thereby freeing a word slot in the FIFO to receive the pending write. Alternatively, the interrupt may require a more intrusive response by the device, such as a system reset ~~resent~~. Without these types of intervention, valid data in the FIFO can be overwritten and thereby provide erroneous results that are derived from the newer data as opposed to the older yet valid data that was overwritten.

On page 8, please replace paragraph **[0030]** with the following amended paragraph:

[0030] Figure 1 illustrates a block diagram of a data storage system designated generally at 10 according to the preferred embodiments. In one preferred embodiment, system 10 is constructed using a single integrated circuit and, indeed, additional circuitry is likely

included within such an integrated circuit. However, to simplify the present illustration and discussion, such additional circuitry is neither shown nor described. Moreover, system 10 may be implemented in connection with numerous digital data systems, where one preferred implementation is detailed later in connection with Figure 4A.

On pages 18-19, please replace paragraph **[0049]** with the following amended paragraph:

[0049] Another observation relating to the preferred embodiments is made by returning to Figures 2I and 2J; recall that those two Figures illustrate the reading of the horizontally stored words in overflow block B_1 (i.e., WD_6 through WD_{13}). However, as each of those words is read, the last four bits of each such word has been overwritten by the vertically stored words in overflow block B_1. Thus, to the extent that the particular bits in the vertically-stored words differ from the bit values of the pre-existing horizontally-stored words, then the accuracy of the data in the last four bits of those horizontally-stored words is compromised. Nonetheless, the accuracy of the more significant bits in the horizontally-stored words is maintained because those bits are not overwritten; thus, the preserved more significant bits may be read and used by the overall system that is relying on such data. The tolerance of a system's ability to use only these more significant bits is dependent on the type of system, and may well be acceptable in certain applications where greater precision is unnecessary. For example, in some audio applications, a temporary loss of data precision of this type may be acceptable. As another example and as further illustrated below, in certain screen data traces, a minor deviation in the screen display may occur as a result of the loss of precision, but this may be an acceptable tradeoff as compared to a large deviation or a system interrupt due to a FIFO overflow condition. Still further, note that the extent of the loss in accuracy may be adjusted in alternative embodiments by changing the ratio of the number of bits used for vertical storage in a block. In other words, in the above-described preferred embodiment, half of the bits (e.g., four of the eight bits) are used to store vertical words, thereby

compromising the data accuracy of the lower half of the horizontally-stored valid words in the overflow block. However, if greater precision is preferred for the horizontally-stored valid words in the overflow block, then a fewer number of the LSBs of those words can be used for vertical storage; thus, in the preceding case, by way of example, the vertical words could be stored only in bit positions BP[0] and BP[1]; in that case, the upper six MSBs of the horizontally stored valid words in the overflow block are preserved, thereby providing greater precision in those words as they are read from FIFO 12. Indeed, numerous other examples may be ascertained by one skilled in the art whereby a different number of least significant bits are overwritten. The specific number of overwritten bits may be a user-provided parameter and/or ~~parameter , and/or~~ it may depend on various application-specific parameters, including the number of horizontal bits available for the storage of each FIFO word (where eight such bits are shown in the preceding example).

On pages 23-24, please replace paragraph **[0062]** with the following amended paragraph:

[0062] In step 220, having been reached because read pointer PTR_{RD} is pointing to an overflow block, system 10 determines whether the horizontal word then indicated by read pointer PTR_{RD} is valid. If so, then method 30 continues from step 220 to step 222, where the horizontal word is read and marked invalid; an example of this instance was described earlier above in connection with Figure 2J and the ~~he~~ reading of word WD_6. Thereafter, method 30 continues from step 222 to step 208, which is described above. Returning to step 220, if the horizontal word then indicated by read pointer PTR_{RD} is invalid, then method 30 continues from step 220 step 230.